WHAT IS CLAIMED IS:

1. A method of manufacturing a microelectronic device, comprising:

providing a substrate including a plurality of doped regions;

forming a patterned feature located over the substrate, the patterned feature including at least one electrode; and

forming a sill located within the electrode, the sill including at least one monolayer of compound and adapted for modifying an electrical property of at least one member adjacent the electrode.

2. The method of claim 1 wherein the sill is formed prior to the patterning of the electrode.

3. The method of claim 1 wherein the sill is formed in the electrode, the electrode and partially etched to reduce the thickness of the electrode and the sill.

4. The method of claim 1 wherein the sill comprises at least two distinct and segregated impurities.

5. The method of claim 1 wherein the substrate comprises diamond.

6. The method of claim 1 wherein the substrate comprises strained silicon.

7. The method of claim 1 wherein the impurity comprises germanium.

8. The method of claim 1 wherein the electrode impurity concentration ranges between about 1×10^{13} atoms/cm^3 and about 1×10^{19} atoms/cm^3.

9. The method of claim 1 wherein the sill is formed through ion implantation.

10. The method of claim 1 wherein the sill is formed through plasma source ion implantation.

11. The method of claim 1 wherein the sill comprises silicon germanium.

12. The method of claim 1 wherein the sill comprises strained silicon.

13. The method of claim 1 wherein the second sill comprises diamond.

14. The method of claim 1 wherein forming the electrode includes depositing a material selected from the group consisting of:

a metal oxide;

polysilicon; and

metal silicide.

15. The method of claim 1 wherein forming the electrode includes depositing a material selected from the group consisting of:

a metal oxide;

a refractory metal; and

metal silicide.

16. A method of manufacturing a microelectronic device, comprising:

providing a substrate including a plurality of doped regions;

forming a patterned feature located over the substrate, the patterned feature including at least one electrode, wherein the electrode is located over a channel region, the channel region located over an insulator located below the channel region and interposing at least two doped regions, the insulator comprised substantially of air; and

forming a sill located within the electrode, the sill including at least one monolayer of compound and adapted for modifying an electrical property of the channel region adjacent the electrode.

17. A microelectronic device, comprising:

a substrate;

a patterned feature located over the substrate and over a plurality of doped regions, the patterned feature comprising at least one electrode, the electrode being situated proximate a plurality of doped layers; and

a sill located within the electrode, the sill comprising at least one impurity and adapted for modifying an electrical property of at least one member adjacent the electrode.

18. The microelectronic device of claim 17 wherein the sill is formed prior to the patterning of the electrode.

19. The microelectronic device of claim 17 wherein the sill is formed in the electrode, the electrode and partially etched to reduce the thickness of the electrode and the sill.

20. The microelectronic device of claim 17 wherein the sill comprises at least two distinct and segregated impurities.

21. The microelectronic device of claim 17 wherein the substrate comprises diamond.

22. The microelectronic device of claim 17 wherein the substrate comprises strained silicon.

23. The microelectronic device of claim 17 wherein the impurity comprises germanium.

24. The microelectronic device of claim 17 wherein the electrode impurity concentration ranges between about 1×10^{13} atoms/cm^2 and about 1×10^{19} atoms/cm^2.

25. The microelectronic device of claim 17 wherein the sill comprises silicon germanium.

26. The microelectronic device of claim 17 wherein the sill comprises strained silicon.

27. The microelectronic device of claim 17 wherein the second sill comprises diamond.

28. A microelectronic device, comprising:

a substrate including a plurality of doped regions;

a patterned feature located over the substrate, the patterned feature including at least one electrode, wherein the electrode is located over a channel region, the channel region located over an insulator located below the channel region and interposing at least two doped regions, the insulator comprised substantially of air; and

a sill located within the electrode, the sill including at least one monolayer of compound and adapted for modifying an electrical property of the channel region adjacent the electrode.

29. An integrated circuit device, comprising:

a substrate;

a plurality of microelectronic devices, each comprising:

a patterned feature located over the substrate and a plurality of doped regions, the patterned feature comprises at least one electrode, the electrode proximate a plurality of doped layers, and

a sill located within the electrode, the sill comprising at least one impurity and adapted for modifying an electrical property of at least one member adjacent the electrode; and

a plurality of interconnect layers for electrically interconnecting the plurality of microelectronic devices.

30. The integrated circuit device of claim 29 further comprising a second sill located below the first sill and proximate the electrode.

31. The integrated circuit of claim 30 wherein the first sill is removed to provide a silicon-on-nothing (SON) substrate, the SON substrate comprising the second sill, a dielectric layer, and the substrate.

32. The integrated circuit device of claim 29 wherein the substrate is diamond.

33. The integrated circuit device of claim 29 wherein the substrate is strained silicon.

34. The integrated circuit device of claim 29 wherein the substrate is strained silicon germanium.

35. The integrated circuit of claim 29 wherein the microelectronic device is a FinFET.

36. The integrated circuit of claim 35 wherein the electrode comprises at least one portion having the sill.

37. The integrated circuit of claim 35 wherein the sill substantially occupies the electrode, the sill occupying portions remote of a channel of the FinFET.

38. An integrated circuit device, comprising:

a substrate;

a plurality of microelectronic devices, each comprising:

a patterned feature located over the substrate, the patterned feature including at least one electrode, wherein the electrode is located over a channel region, the channel region located over an insulator located below the channel region and interposing at least two doped regions, the insulator comprised substantially of air, and

a sill located within the electrode, the sill including at least one monolayer of compound and adapted for modifying an electrical property of the channel region adjacent the electrode; and

a plurality of interconnect layers for electrically interconnecting the plurality of microelectronic devices.